Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A system for processing an input signal, the system comprising:

- an adaptive predistortion subsystem for receiving said input signal and for producing a predistorted signal by applying a deliberate predistortion to said input signal;

- a signal processing subsystem receiving and processing said predistorted signal and producing a system output signal;

- a feedback signal processing subsystem for receiving and processing a feedback signal derived from said system output signal; and

- a delay subsystem for providing a delay to a replica of said input signal to produce a delayed signal, said delayed signal being used by said adaptive predistortion subsystem and said feedback processing subsystem,

wherein

- said adaptive predistortion subsystem distorts said input signal to compensate for distortions in said system output signal;

- said signal processing subsystem decomposes said predistorted signal into separate components, each of said separate components being processed separately;

- said processing subsystem combines said components after processing to produce said system output signal;

- an output of said feedback processing subsystem being used by said adaptive predistortion subsystem;

- said deliberate predistortion applied to said input signal by said adaptive predistortion subsystem to produce said predistorted signal is adjusted based on said system output signal;

- said predistortion subsystem is controlled by a preprogrammed control device.

2. (Original) A system according to claim 1 wherein said signal processing subsystem comprises:

- a signal decomposer for decomposing said predistorted signal into at least two components;

- at least two signal component processor blocks, each signal processor block receiving an output of said signal decomposer and each signal processor block separately processes said output received from said signal decomposer; and

- a combiner receiving a processed output from each of said at least two signal component processor blocks, said combiner producing said system output signal from said processed outputs of said at least two signal component processor blocks.

3. (Original) A system according to claim 2 wherein at least one of said at least two signal component processor blocks includes an amplifier.

4. (Original) A system according to claim 3 wherein said amplifier is a non-linear amplifier.

5. (Original) A system according to claim 1 wherein said system is part of a signal transmission system.

6. (Original) A system according to claim 1 wherein at least some of said distortions are due to said combiner.

7. (Original) A system according to claim 3 wherein said amplifier is a switch mode amplifier.

8. (Original) A system according to claim 3 wherein said amplifier has a low output impedance.

9. (Original) A system according to claim 1 wherein said deliberate predistortion includes magnitude distortions which adjust a magnitude of said input signal.

10. (Original) A system according to claim 1 wherein said deliberate predistortion includes phase distortions which adjust a phase of said input signal.

11. (Original) A system according to claim 1 wherein said deliberate predistortion is based on at least one entry in a lookup table.

12. – 18. (Cancelled).

12 ~~19.~~ (Original) A system according to claim 1 wherein said predistortion subsystem receives a replica of said system output signal.

13 ~~20.~~ (Original) A system according to claim 2 wherein said deliberate predistortion is dependent on differences between said input signal and said replica of said system output signal.

14 ~~21.~~ (Original) A system according to claim 11 wherein entries in said lookup table are periodically updated based on characteristics of a replica of said system output signal.

15 ~~22.~~ (Original) A system according to claim 11 wherein said deliberate predistortion is based on an interpolation of entries in said table.

16 ~~23.~~ (Original) A system according to claim 1 wherein said predistortion subsystem includes:

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- determining means for determining said deliberate predistortion;
- adjustment means for applying said deliberate predistortion to said input signal;
- update means for periodically updating said determining means based on said system output signal.

17 ~~24.~~ (Original) A system according to claim 16 ~~23~~ wherein said adjustment means receives parameters of said deliberate predistortion from said determining means.

25. – 31. (Cancelled).

18 ~~32.~~ (Original) A system according to claim 1 wherein said delay subsystem comprises:

- a plurality of delay elements;

- means for sampling said input signal;
- means for storing samples of said input signal;
- means for selecting selected samples of said input signal; and
- means for combining said selected samples of said input signal.

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33. (Original) A system according to claim 1 wherein said delay subsystem comprises separate subsystems for separately delaying a magnitude and a phase of said input signal.

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34. (Original) A system according to claim 1 wherein said feedback signal processing subsystem comprises means for adjusting a phase of a replica of said system output signal.

35 – 37. (Cancelled).

(cancelled)

38. (Withdrawn). A method of initializing a phase correction to be applied to a feedback signal, said feedback signal to be used in determining a deliberate predistortion for a signal processing system, the method comprising:

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a) initiating a coarse delay search

b) selecting a time window of W samples of said feedback signal and an input signal with a predetermined sample delay increments of δ between samples

c) calculating an inner product P_δ by performing a complex multiply and accumulate process for the W samples in the time window

d) storing a maximum $|P_\delta|$ found

e) repeating steps c) and d) for subsequent time windows and incrementing δ by a predetermined amount for each time window

f) repeating steps b) - e) for a fine delay search using fractional sample increments to cover a predetermined delay range, said delay range being centered on a maximum delay increment δ_{max} found during said coarse delay search.

(cancelled)

39. (Withdrawn). A method according to claim 38 wherein said inner-product process is ~~defined by~~

$$P_\delta = A_{MAC} \cdot \sum_{k=n\cdot W}^{n\cdot W+W-1} \exp(j \cdot (\angle x_\delta(k) - \angle z(k)))$$

where

$\angle x_\delta(k)$ is a phase of said input signal

$\angle z(k)$ is a phase of said feedback signal

A_{MAC} is a constant

n is an integer denoting a time window

(cancelled)

40. (Withdrawn). A method according to claim 38 wherein said phase correction is a phase of said maximum P_δ.

41 – 44. (Cancelled).

21 45. (Original) A system according to claim 1 wherein said predistorted signal is adjusted based on said system output signal and said input signal.

46. (Cancelled).

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22 47. (Original) A system according to claim 23 16 wherein said update means periodically updates said determining means based on said system output signal and said input signal.

(cancelled)

48. (Withdrawn) A method according to claim 38 wherein said inner product P_δ is based on a phase of said input signal and on a phase of a system output signal.

23 49. (Original) A system according to claim 1 wherein said adaptive predistortion subsystem includes a distortion monitor for monitoring an amount of distortion in said system output signal.

24 ~~50.~~ (Original) A system according to claim ~~49~~ 23 wherein said distortion monitor generates an alarm when said distortion exceeds a predetermined level.

25 ~~51.~~ (Original) A system according to claim ~~23~~ 16 wherein said predistortion subsystem protects against subsystem instability by only updating said determining means in specific predetermined instances.

26 ~~52.~~ (Original) A system according to claim 1 wherein said control device is programmed with a predefined set of states, each state having associated with it a predefined set of commands to be executed by said subsystem when said device is in said state.

27 ~~53.~~ (Original) A system according to claim 1 wherein said predistortion subsystem operates based on a duty cycle such that said subsystem is operating only a fraction of the time.

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28 ~~54.~~ (Original) A system according to claim ~~53~~ 27 wherein said duty cycle is determined by said control device.

29 ~~55.~~ (Original) A system according to claim ~~23~~ 16 wherein said update means updates said determining means based on a duty cycle determined by said control device.

30 ~~56.~~ (Original) A system according to claim ~~23~~ 16 wherein said adaptive predistortion subsystem initializes itself based on a duty cycle dependent on a number of updates by which said update means updates said determining means.

31 ~~57.~~ (Original) A system according to claim 1 wherein said control device comprises:

- a processor means for receiving and processing data relating to a status of said subsystem;
- a first memory means for storing said data; and
- a second memory means for storing preprogrammed settings for said device.

32 ~~58.~~ (Original) A system according to claim 1 wherein said device controls an update duty cycle for said predistortion subsystem, said update duty cycle being determinative of how often said predistortion subsystem updates at least one internal lookup table.

33 ~~59.~~ (Original) A system according to claim 1 wherein said control device controls an initialization duty cycle for said predistortion subsystem, said initialization duty cycle being determinative of how often said predistortion subsystem initializes itself.

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34 ~~60.~~ (Original) A system according to claim ~~59~~ 33 wherein said initialization duty cycle is dependent on how often said predistortion subsystem updates at least one internal lookup table.

35 ~~61.~~ (Original) A system according to claim ~~49~~ 23 wherein said control device switches from one state to another based on input from said distortion monitor which monitors a level of distortion for said subsystem.